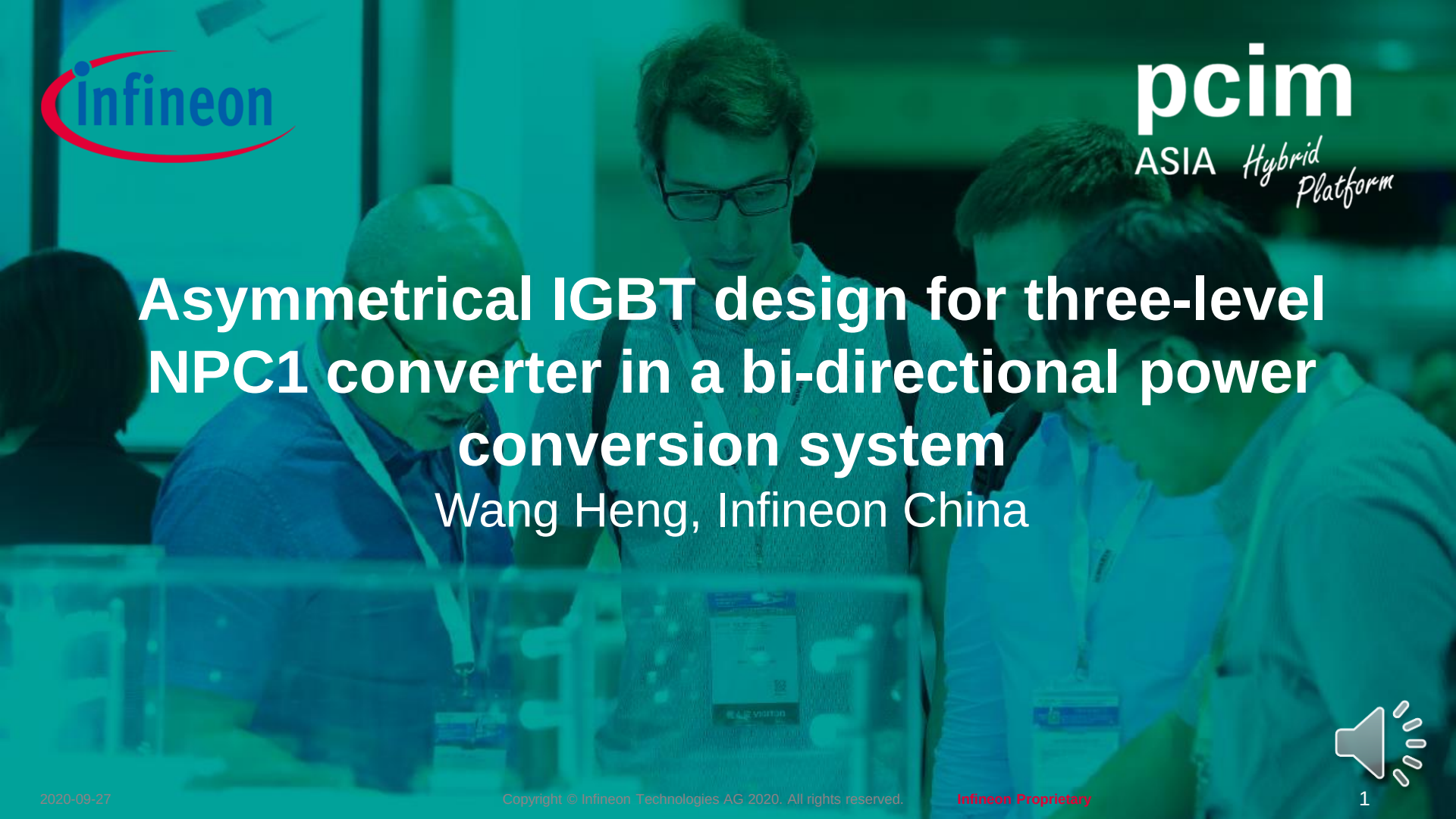


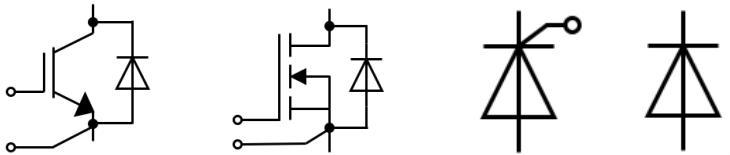
Asymmetrical IGBT design for three-level NPC1 converter in a bi-directional power conversion system

Wang Heng, Infineon China

speaker

- **Name:** Wang Heng
- **Company:** Infineon China
- **Position:** Field Application Engineer

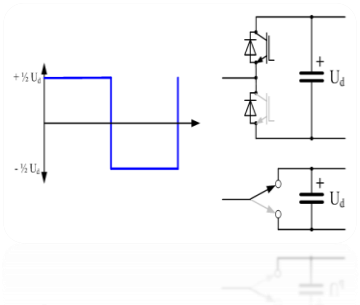
- **Background**
  - Bachelor / Master degree in Electrical Engineering
  - R&D engineer in Emerson
  - FAE in Infineon since 2010

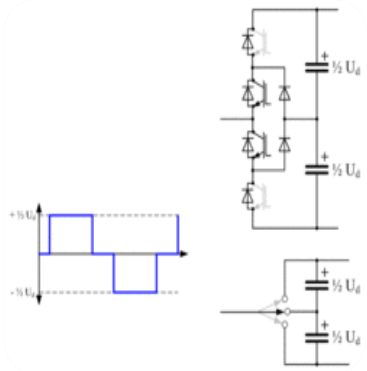


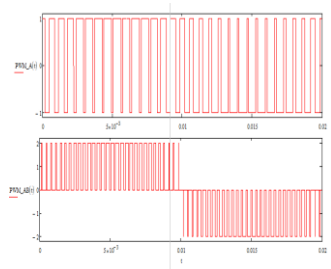
Contents

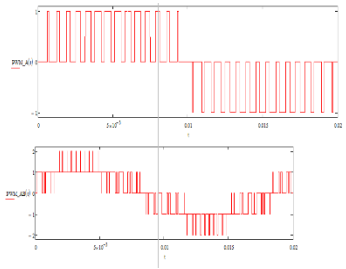
1. Basics of NPC1 topology

- **2L vs 3L**







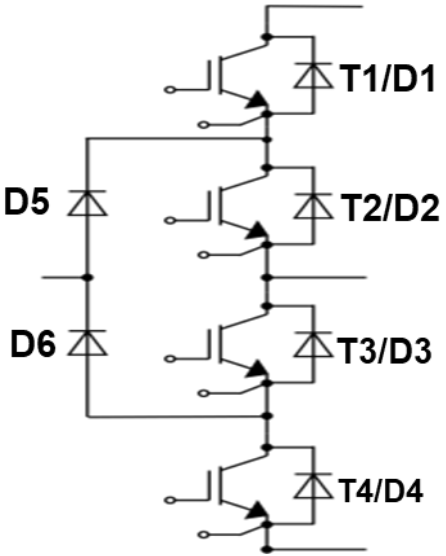


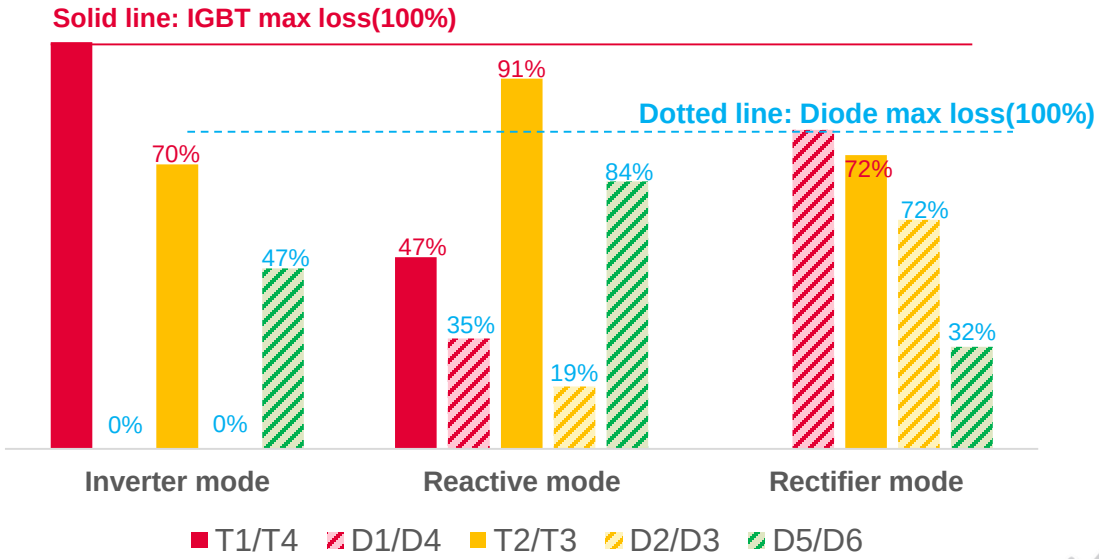
Benefits from 3L – NPC1 topology:

1. *Be able to work under higher DC bus voltage*
2. *Reduction of losses and improvement of system efficiency*
3. *Higher equivalent switching frequency and smaller output filters*
4. *Improved EMC performance*
5. *Use of low-voltage device to replace high-voltage device (reduces system cost)*

1. Basics of NPC1 topology

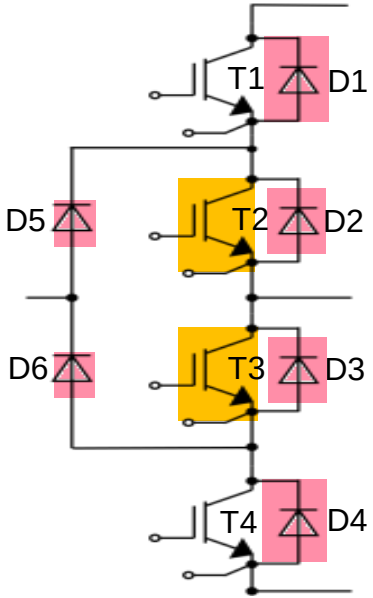
› Typical distribution of power losses in inverter mode, reactive mode, and rectifier mode.



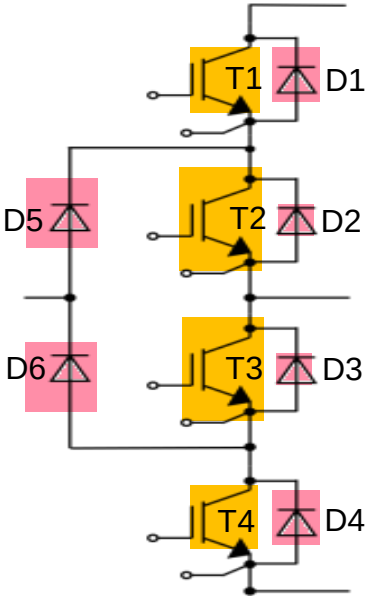


2. The minimum chip area for NPC1 topology

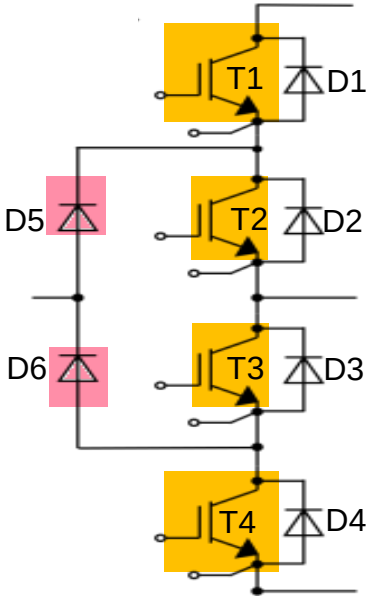
› Draft chip area is normalized by power losses



a) Rectifier mode(cosφ=-1)



b) Reactive mode(cosφ=0)



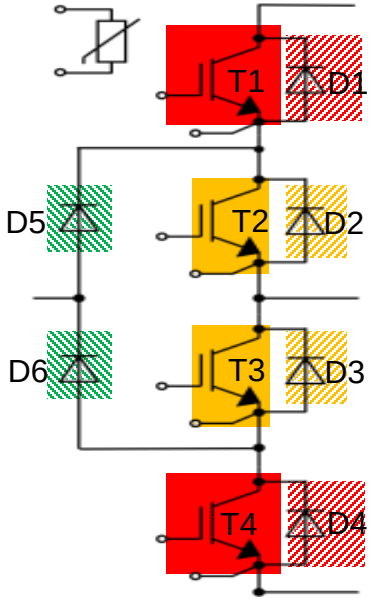
c) Inverter mode(cosφ=1)

2. The minimum chip area for NPC1 topology

- **Design hits for a bi-direction converter**
  - T1/T4: highest losses at inverter mode, both Pcon and Psw
  - D1/D4: highest losses at rectifier mode, both Pcon and Psw
  - T2/T3: highest losses at reactive mode, both Pcon and Psw
  - D2/D3: highest losses at rectifier mode, **only Pcon**
  - D5/D6: highest losses at reactive mode, both Pcon and Psw

  - **Commutation loop**
    - Rectifier & Reactive mode: **Long**
    - Inverter mode (PF=1): **Short**

Typical power losses distribution



Target chip area for bi-direction converter

3. The prototype design

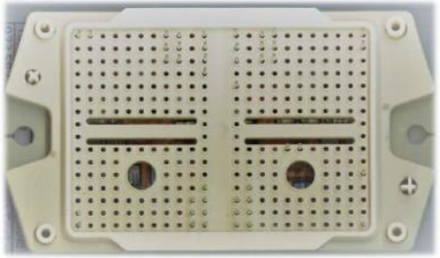
a) Target application
b) Package
c) IGBT/Diode chips
d) Current rating selection

3. The prototype design

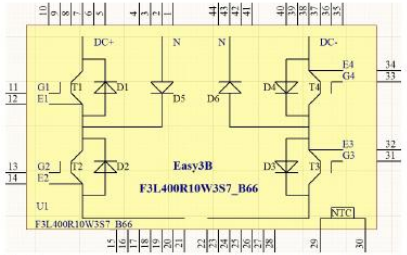
› **Target application:** bi-directional power conversion system, e.g. PCS in Energy Storage System

Power conversion system for energy storage system	
Conditions	**value**
Vdc	1300V
Uout	480V
Power rating	125kW
Switching frequency	16kHz
Line frequency	50Hz
Ta	40℃
cosφ	1,0,-1

› **New package:** Easy3B is a low cost and flexible housing for kinds of topology, and enables customized pinout.



(a) Easy 3B Module vertical view

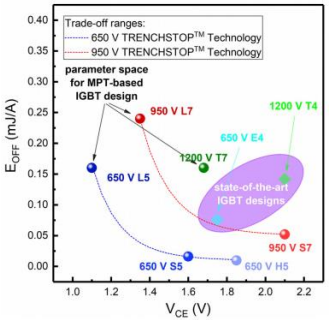


(b) Power module pinout sketch map

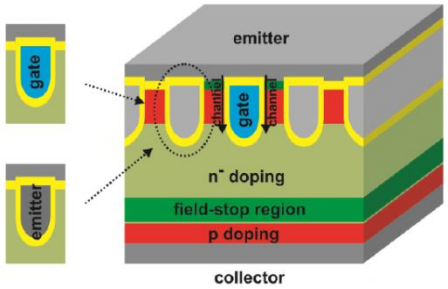
3. The prototype design

› **New Chip:** latest 7th generation 950V fast switching IGBT(S7), covering a wide range of DC-link voltages from 500 V to 1300 V for long term operating.

IGBT7

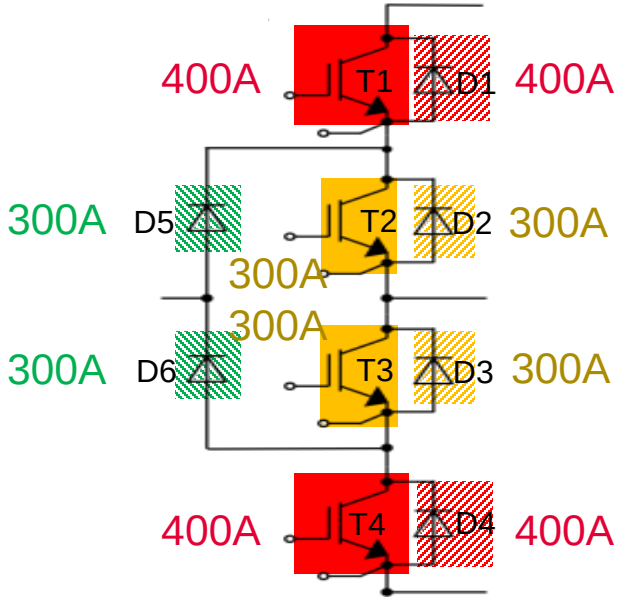


Source: PCIM-2019



Source: PCIM-2018

› **Configuration:** current rating



Proposed current rating for each switch

4. Experimental verification

a) layout checking
b) switching test
c) thermal performance
d) electrical measure

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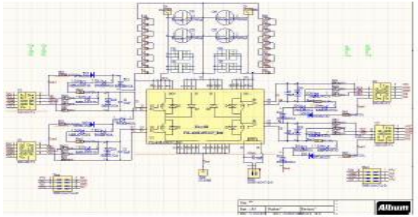
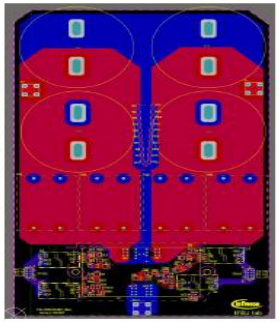
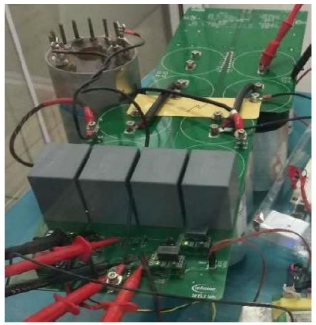
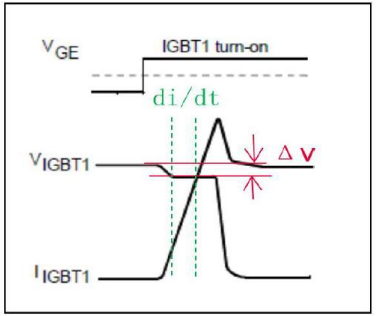
› Set up for Ls measurement





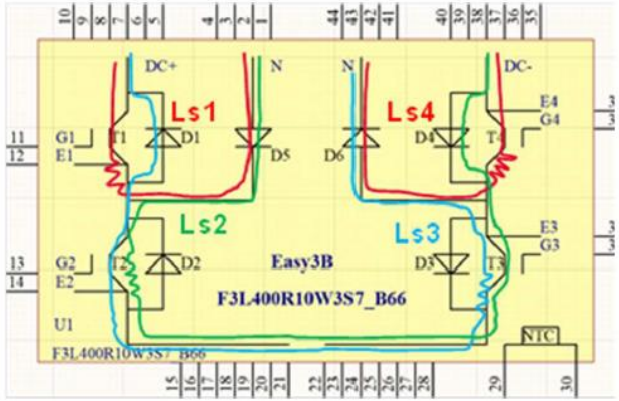




$$L_s = \frac{\Delta V}{di/dt}$$

› Ls value for each commutation loop

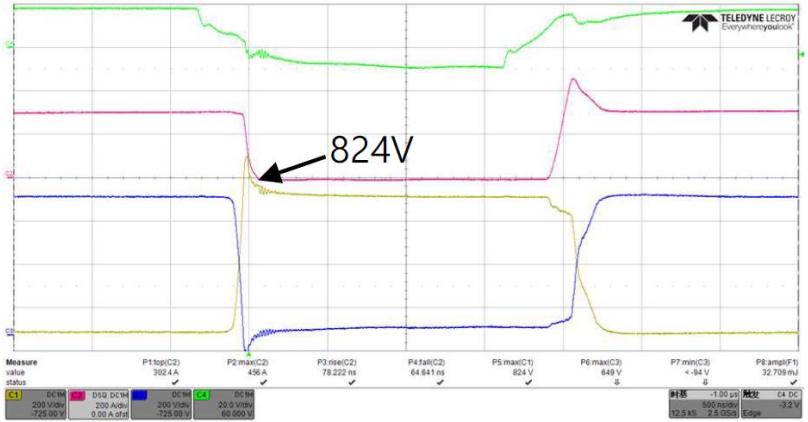
- Ls1: **T1**-**D1**
- Ls2: (D5)-**T2**-(T3)-**D4**
- Ls3: **D1**-(T2)-**T3**-(D6)
- Ls4: **T4**-**D6**



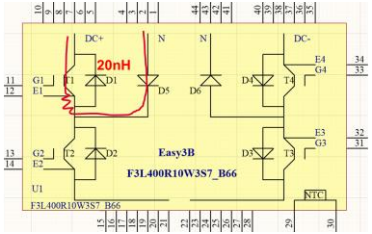
Note: Ls1 is not equal to Ls4 due to different chip positions, as well as Ls2 and Ls3.

4. Experimental verification - switching test

› Switching with Ls1/Ls4



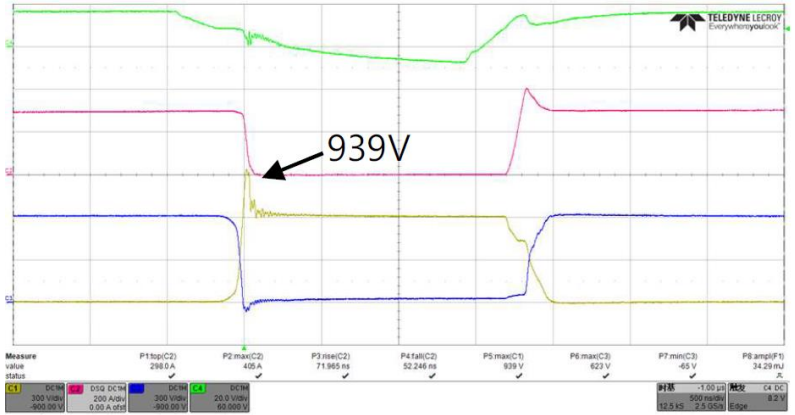
a) Short loop



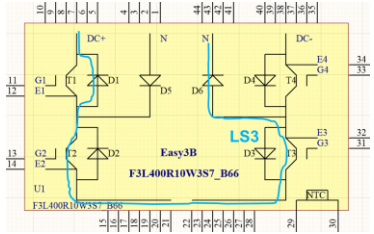
With smaller Ls:

- Lower spike voltage
- Reverse recovery peak power is smaller

› Switching with Ls2/Ls3



b) Long loop



With larger Ls:

- High spike voltage
- Worse reverse recovery
- Easy in snap-off

4. Experimental verification - thermal performance

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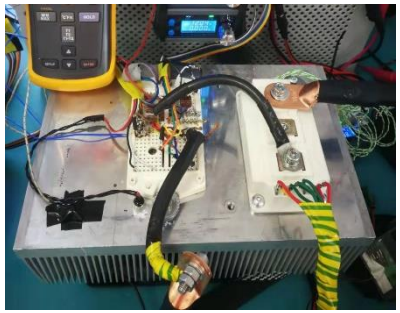
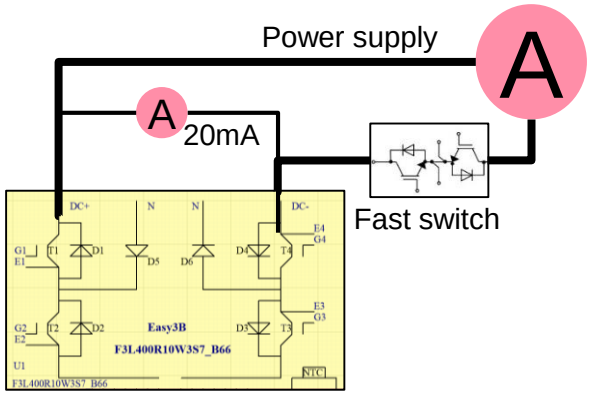
› Zth measurement

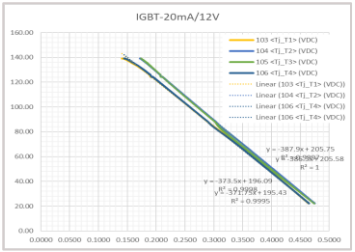


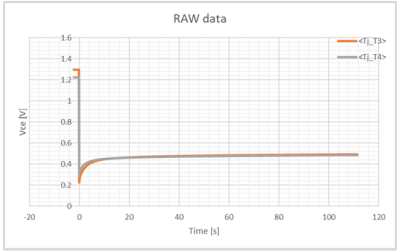


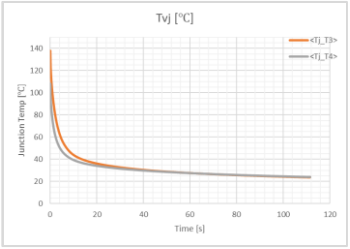
Test method refer to JESD51

Calibration -> Thermal measure -> Math Calculation

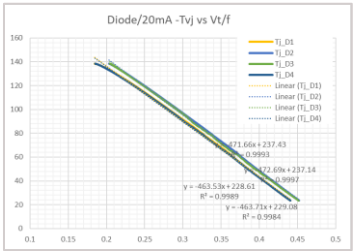
IGBT

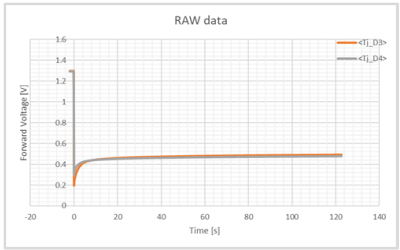


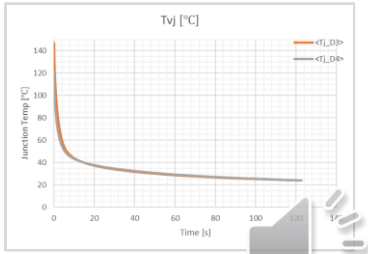




Diode

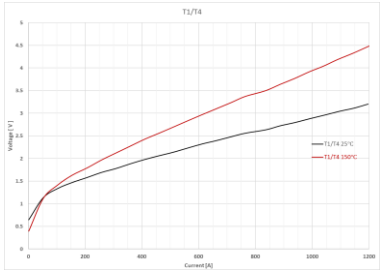




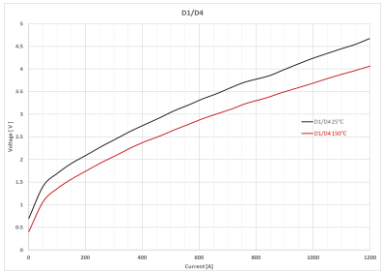


› Conduction loss

– IGBT-V/I

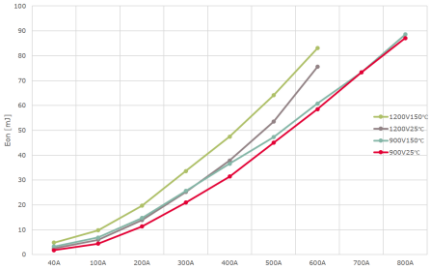


– Diode-V/I

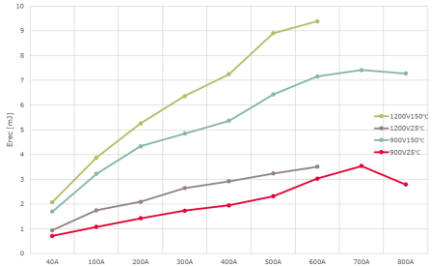


› Switching loss

› IGBT-Eon

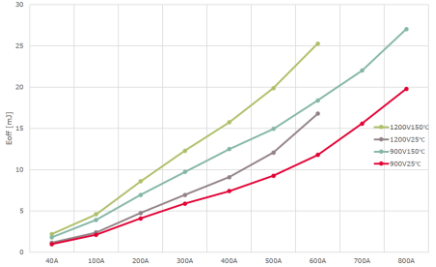


› Diode-Erec



› Switching loss

› IGBT-Eoff



From such measure results ->
to build up accurate device models for simulation

5. Simulation
- power losses and junction temperature

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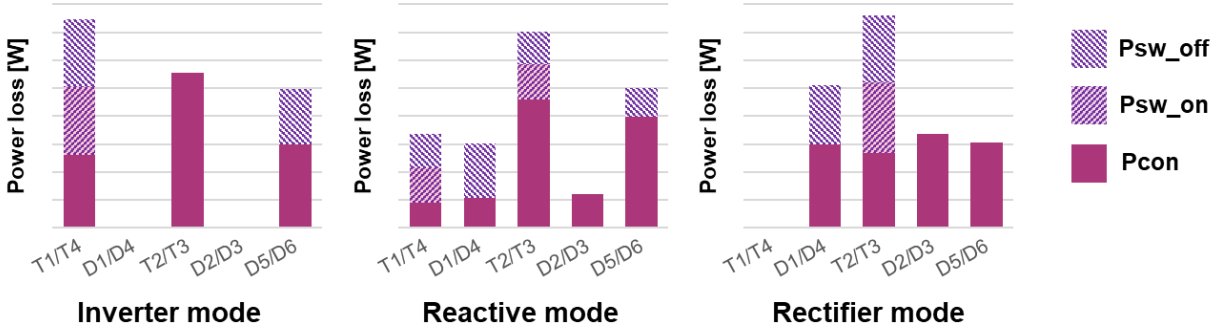
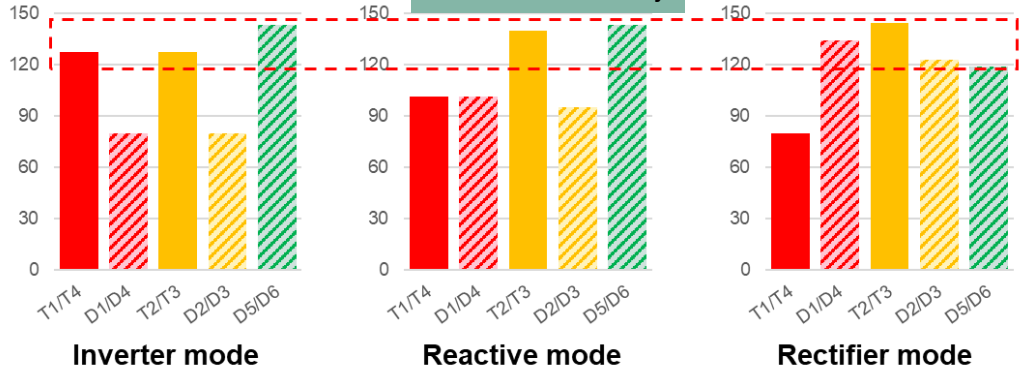
› Simulation results:

Power conversion system for energy storage system	
Conditions	**value**
Vdc	1200V
Uout	480V
Power rating	125kW
Switching frequency	16kHz
Line frequency	50Hz
Ta	40℃
cosφ	1,0,-1

Power losses distribution



The maximum Tvj



6. Conclusion

- NPC1 topology is suggested to apply asymmetrical design based on its features.
- A prototype is designed based on minimum chip area concept, and the device is simulated by accurate model from switching and thermal test data.
- Simulated results show the Tvjmax are at the same level at around 140℃ in different operation modes. The 2nd and 3rd hottest temperatures are also checked as the indicator for module evaluation.
- A novel IGBT module saves costs from a tailored chip area and to be a best cost-performance solution.

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